IV Year I Semester   **L   T   P   C**

Code: 17EC703   **3   1   0   3**

VLSI DESIGN

Unit I:
Introduction and Basic Electrical Properties of MOS Circuits: Introduction to IC technology, Fabrication process: nMOS, pMOS and CMOS. Ids versus Vds Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor Trans, Output Conductance and Figure of Merit. nMOS Inverter, Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter, and through one or more pass transistors. Alternative forms of pull-up, The CMOS Inverter, Latch-up in CMOS circuits, Bi-CMOS Inverter, Comparison between CMOS and BiCMOS technology.

Unit II:
MOS and Bi-CMOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout, General observations on the Design rules, 2µm Double Metal, Double Poly, CMOS/BiCMOS rules, 1.2µm Double Metal, Double Poly CMOS rules, Layout Diagrams of NAND and NOR gates and CMOS inverter, Symbolic Diagrams-Translation to Mask Form.

Unit III:
Basic Circuit Concepts: Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters, Area Capacitance of Layers, Standard unit of capacitance, Some area Capacitance Calculations, The Delay Unit, Inverter Delays, Driving large capacitive loads, Propagation Delays, Wiring Capacitances, Choice of layers.
Scaling of MOS Circuits: Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling, Limits due to sub threshold currents, Limits on logic levels and supply voltage due to noise and current density. Switch logic, Gate logic.

Unit IV:
Chip Input and Output circuits: ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip clock Generation and Distribution.
Design for Testability: Fault types and Models, Controllability and Observability, Ad Hoc Testable Design Techniques, Scan Based Techniques and Built-In Self Test techniques.

Unit V:
FPGA Design: FPGA design flow, Basic FPGA architecture, FPGA Technologies, FPGA families- Altera Flex 8000FPGA, Altera Flex 10FPGA, Xilinx XC4000 series FPGA, Xilinx Spartan XL FPGA, Xilinx Spartan II FPGAs, Xilinx Vertex FPGA. Case studies: FPGA Implementation of Half adder and full adder.
Introduction to synthesis: Logic synthesis, RTL synthesis, High level Synthesis.

Unit VI:

Introduction to Low Power VLSI Design: Introduction to Deep submicron digital IC design, Low Power CMOS Logic Circuits: Over view of power consumption, Low –power design through voltage scaling, Estimation and optimization of switching activity, Reduction of switching capacitance. Interconnect Design, Power Grid and Clock Design.

Text Books:

1. Essentials of VLSI Circuits and Systems - Kamran Eshraghian, Douglas and A. Pucknell and Sholeh Eshraghian, Prentice-Hall of India Private Limited, 2005 Edition.
2. CMOS Digital Integrated Circuits Analysis and Design- Sung-Mo Kang, Yusuf Leblebici, Tata McGraw-Hill Education, 2003.

References:

1. Advanced Digital Design with the Verilog HDL, Michael D.Ciletti, Xilinx Design Series, Pearson Education
2. 2. Analysis and Design of Digital Integrated Circuits in Deep submicron Technology, 3'rd edition, David Hodges.