IV B.Tech – I Semester

(20EC7726) COMPUTER SYSTEMS ARCHITECTURE AND ORGANIZATION
(Minors)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
30	70	100	3	1	0	4

Pre-Requisites: Digital Electronics

Course Objectives:

- Discuss the basic concepts and structure of computers.
- Explain different types of addressing modes and memory organization.
- Understand concepts of register transfer logic and arithmetic operations.
- Summarize the Instruction execution stages.
- Learn the different types of serial communication techniques.

UNIT I: Digital Computers

Digital Computers: Introduction, Block diagram of Digital Computer, Definition of Computer Organization, Computer Design and Computer Architecture. Register Transfer Language and Micro operations: Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit. Basic Computer Organization and Design: Instruction codes, Computer Registers, Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt.

UNIT II: Data Representation

Data types, Complements, Fixed Point Representation, Floating Point Representation. Computer Arithmetic: Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations.

UNIT III: Microprogrammed Control

Control memory, Address sequencing, micro program example, design of control unit. Central Processing Unit: General Register Organization, Instruction Formats, Addressing modes, Data Transfer and Manipulation, Program Control.

UNIT IV: Reduced Instruction Set Computer

CISC Characteristics, RISC Characteristics. Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processor. Multi Processors: Characteristics of Multiprocessors, Interconnection Structures, Interprocessor arbitration, Interprocessor communication and synchronization, Cache Coherence schemes.

UNIT V: Input-Output Organization

Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt Direct memory Access. Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory.

COURSE OUTCOMES:

After successful completion of the course, the students can be able to

S. No	Course Outcome	BTL
1	Understand the impact of instruction set architecture on cost-performance of computer design.	L2
2	Understand ways to incorporate long latency operations in pipeline design.	L2
3	Design a pipeline for consistent execution of instructions with minimum hazards.	L4
4	Understand dynamic scheduling methods and their adaptation to contemporary microprocessor design.	L2
5	Understand ways to take advantage of instruction level parallelism for high performance processor design.	L2

Correlation of COs with POs & PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	-	-	-	-	-	-	-	-	-	3	-
CO2	3	1	1	-	-	-	-	-	-	-	-	-	3	-
CO3	2	3	2	-	-	-	-	-	-	-	-	-	2	-
CO4	3	3	1	-	-	-	-	-	-	-	-	-	3	-
CO5	2	2	2	-	-	-	-	-	-	-	-	-	2	-

Text Books:

1. Computer System Architecture – M. Moris Mano, Third Edition, Pearson/PHI.
2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky Computer Organization, McGraw-Hill, Fifth Edition, Reprint 2012.
3. John P. Hayes, Computer Architecture and Organization, Tata McGraw Hill, Third Edition, 1998. Reference books.
4. William Stallings, Computer Organization and Architecture-Designing for Performance, Pearson Education, Seventh edition, 2006.

Reference Books:

1. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI.
2. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.
3. Donald e Givone, “Digital Principles and Design”, TMH.