Dr. Y. Sudha Vani

Associate Professor
Department of Electronics & communication Engineering
Raghu Engineering College, Dakamari, Visakhapatnam-531162
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Interests: design of Low Power/voltage SRAM Memory, digital circuits, emerging spin-based memory, Low Power VLSI and logic design and modulo adders beyond CMOS devices.

Course Taught Previously

PG.

- Semiconductor memory devices
- Mixed IC Design
- Digital IC Design

UG.

- Switching Theory and Logic Design
- Digital Logic Design
- VLSI Design
- Digital IC Applications
- Verilog HDL
- EMI
- Electronics Devices and Circuits
- Electronics Circuit Analysis
- Antennas and Wave Propagation

Laboratories Handled

- Digital IC Design Lab
- Verilog HDL Lab
- Electronics Devices and Circuits Lab
- Digital Logic Design Lab
- DICA LAB
- VLSI Design lab

Publications
International Journals

- **Yamani, Sudha Vani**, N. Usha Rani, and Ramesh Vaddi. "Design and Performance Benchmarking of Hybrid Tunnel FET/STT-MTJ-Based Logic In-Memory Designs for Energy Efficiency." ***IEEE Transactions on Magnetics*** 58, no. 4 (2022): 1-11. **(Published- SCI)**

- **Y. Sudha Vani,** N. Usha Rani, and Ramesh Vaddi, "An Energy-Efficient Hybrid Tunnel FET based STT-MRAM memory cell at Low V_{DD}" **international journal of electronics**, Apr 2021, pp,1-16. **(Published- SCIE)**
- **Y. Sudha Vani,** N. Usha Rani, and Ramesh Vaddi, "A 128Kb RAM Design with Capacitor-Based Offset Compensation and Double-Diode based Read Assist Circuits at Low V_{DD}" Journal of Scientific and Industrial Research (JSIR) Sep 2020,79(09), pp-788-793. **(Published-SCI)**
- Kavitha Patcha, Sarada Musala, K. Vijayavardhan, **Y. Sudha Vani** and Avireni Srinivasulu " Carbon Nano Tube Field Effect Transistors Based Ternary Ex-OR and Ex-NOR Gates" *Current Nanoscience,* 2016, *12,* 520-526. **(SCI-indexed)**
- P.RadhikaRamya, **Y.SudhaVani** has published a paper titled "Optimization and Implementation of Reversible BCD Adder in Terms of Number of Lines" in International Journal of Application or Innovation in Engineering & Management (ISSN 2319 – 4847), Volume 2, Issue 9, September 2013.
- B.T.P Madhav, VGKM Pisipati, Anjaneyulu Badugu, **Y.Sudhavani** "performance Investigation of Triangular Toothed Serrated Micro strip Patch Antennas" in International Journal of Emerging Trends in Engineering and Development (IJETED), Issue 2 Vol.4,Pag 178-184, May 2012,ISSN:2249-6149 **.**

Conference Proceedings

- **Y. Sudha Vani,** H K Raghu Vamsi, S. Srinivasa Rao, "Design of Three Stage Dynamic Comparator with Tail Transistor using 20nm FinFET Technology for ADCs" *International Conference on Computing, Communication and Power Technology Organized by Raghu Institute of Technology and Raghu Engineering College* Visakhapatnam in technical collaboration with IEEE Vizag Bay Section, 7-8 January, 2022.
- **Y. Sudha Vani,** N. Usha Rani, and Ramesh Vaddi. "Low Write Energy STT-MRAM Cell Using 2T-Hybrid Tunnel FETs Exploiting the Steep Slope and Ambipolar Characteristics." In *International Symposium on VLSI Design and Test (VDAT)*, pp. 398-405. Springer, Singapore, 2017.
- **Y. Sudha Vani,** N. Usha Rani, and Ramesh Vaddi, "A Low Voltage Capacitor Based Current Controlled Sense Amplifier for Input Offset Compensation" in *14th international SoC design conference (ISOCC)*, Nov 5-7, Seoual, South Korea, 2017 . **(Scopus-indexed)**
- P.RadhikaRamya**, Y.Sudhavani**, R.vijayalakshmi "Implementation of energy efficient and low complex filters with reconfigurability usage",proc. International conference on Navigational systems and signal processing applications"NSSP-2013",in university college of engineering & technology ,acharya nagarjuna university,gutur,A.P,13th& 14th December 2013.

PHDs Supervised: NIL

Workshops/Conferences/Seminars/Symposiums organised: NIL

Visit to outside institute/organization: NIL

Continuing Education / QIP Short Term Lectures / Special Lectures given: NIL

Details of professional training and research experience

National / International	Topic, Venue	Date and Year
Conducted by Other Organizations		
NATIONAL	Two Weeks Workshop On Analog Electronics Conducted By IIT-Kharagpur, ProfananyaDhar	4^{TH}-14^{TH} June 2013
NATIONAL	Capacity Building in the area of Electronic Product Design and Production technology, CDAC, Hyderabad	2^{nd} -7^{th} June 2014
Conducted by Vignan's University		
NATIONAL	Two Days Workshop On System Design Using Xilinx FPGA,Vignan University.	9^{TH} -10^{TH} July 2013
NATIONAL	Six days workshop on Enhancing English Language proficiency in Vignan's university	24^{th}-29^{th} June 2013
NATIONAL	VLSI Design Using Cadence Tool in Vignan's university	9^{th} -11^{th} June 2014
NATIONAL	Recent Trends In communication technologies & Signal Processing in Vignan's university	27^{th} to 28^{th} Sep 2014
NATIONAL	Embedded Systems and wireless Sensor Networks in Vignan's university	18^{th} -19^{th} April 2015
Raghu Engineering College		
NATIONAL	"Advances in Practical Antenna Design" by the E & ICT Academy, NIT Warangal	25^{th} – 30^{th} May 2017
NATIONAL	Real Time Embedded Systems and IoT, its Applications" by NIT Warangal	2^{nd} - 8^{th} June 2018
NATIONAL	"Quality Enhancement in Curriculum Design and Development for Higher Education Institutes" by IQAC, REC	29^{th} & 30^{th} Nov 2018
NATIONAL	"Design Challenges in Deep Sub-Micron Technology" by RIT	5^{th} – 19^{th} Aug 2019
NATIONAL	"Advanced Signal Processing, Communications using AI and ML Techniques" by GMR Institute of Technology and Sri Sairam Institute of Technology	21^{st} - 25^{th} March, 2022
NATIONAL	"Machine Learning in Real Time Embedded & IOT Applications" by NIT Warangal& REC	2^{nd} – 12^{th} May 2022
NATIONAL	Professional Development Programme on "Accreditation and Outcome Based Education"	19^{th} – 23^{rd} July 2022
NATIONAL	"Inculcating Universal Human Values in Technical Education" organized by All India Council for Technical Education (AICTE)	19^{th} – 23^{rd} Sep 2022

Projects Sponsored R & D, Consultancy Projects: NIL

Awards and Honors

- I got the Elite-silver in NPTEL Course- System Design Through verilog
- I got the top 5% in NPTEL online course- Digital Electronics
- I got Appreciation certification from Chairman, Raghu Engineering College for best performance in NPTEL, 2019.
- I got Appreciation certification from Chairman, Vignan's Group for 100% result in 2013.

Additional Responsibility

RESPONSIBILITIES WITHIN THE INSTITUTE:

- NAAC criteria-1 overall Coordinator
- College level Women's Grievance cell Convener
- Sent SMS to daily absentees
- Exam cell duties
- Result analysis of all years
- Simulation Lab In-charge
- NBA-Criteria P4(result analysis)

POSITIONS HELD OUTSIDE THE INSTITUTE:

- Acting as a In-charge of 2009 Batch students in ECE department, CHEC, Chebrolu.
- Acting as Time Table In charge for ECE department, CHEC, Chebrolu.

In Vignan's University:

- Acting as coordinator of Dept. BOS(ECE).
- Acting as dept. TIME TABLE In-Charge.
- Involved in NAAC work
- Natraj event coordinator for Mahostav'13 & 14.
- Acting as class teacher of 2010 batch (III-II ECE-A).
- Acting as class teacher of 2011 batch (III-I ECE-D).